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Isolated Flyback Converter Designing, Modeling and Suitable Control Strategies

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***Abstract*— This paper addresses a novel approach for designing and modeling of the isolated flyback converter. Modeling is done without parasitic as well as with parasitic components. A detailed analysis, simulation and different control strategy are conferred for flyback converter in continuous conduction mode (CCM). To verify the design and modeling at primary stage, study of the converter is practiced in CCM operation for input AC voltage 230V at 50Hz and output DC voltage of 5V and 50W output power rating using PSIM 6.0 software. Simulation result shows a little ripple in output of the converter in open loop. Finally in order to evaluate the system as well as response of the controller, flyback converter is simulated using MATLAB. This work, highlighting the modeling when the system have transformer and facilitate designers to go for it when they need one or more than one output for a given application upto 150W .**

***Index Terms*— Flyback converter, Average model, Non-minimum phase, Design, Analysis and Result.**

I. INTRODUCTION

Electronic circuits which use integrated-circuits (IC) need a standard DC voltage of fixed magnitude which generally vary between -18 to +18 volts. In some electronic equipments one may need multiple output power supplies. For example, in a Personal Computer (PC) one may need ±5 volt and ±12 volt power supplies. These DC power supplies are generally provided from the standard power source i.e. AC voltage of 115V / 60Hz or 230V / 50Hz. For low output power applications the most preferred converter is flyback, the advantage of this converter is that the output state and the input main supply are completely isolated. Ref. [5] the circuit topology of flyback converter is simplest if we compare it with other SMPS circuits. The input given to the converter is generally unregulated dc voltage which is obtained by rectifying the ac voltage followed by a capacitor filter (it can be realized by fig. 7). Flyback converters use a transformer so that they can give single or multiple isolated output voltages. Ref. [9] but if we talk about energy efficiency (η), fly-back converter is not good as compared with other SMPS circuits though its topology is very simple. Flyback can be operated in two different modes:

1. Continuous conduction mode (CCM)
2. Discontinuous conduction mode (DCM)

Ref. [1] if the application demands high voltage and low current output then DCM is mostly recommended. Meanwhile, CCM is recommended for low voltage and high current output applications. Application we are

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dealing with is low voltage and high current, so we have gone with CCM. This paper presents a simple methodology to design flyback converter with parasitic components. Although the impact of parasitic components may be negligible in low-power applications, but when the load resistance becomes considerably small, the effects of these parasitic elements cannot be ignored. Our approach starts with AC input of 230V which is converted to unregulated DC voltage and then supplied to the converter circuit. Ref. [6] flyback converter provides multiple isolated outputs and therefore it is the preferred topology for industrial applications.

In this paper a basic concept of linear circuit is used to model the converter. Because of switching characteristics the converter is not a linear system and to apply linear control strategy the system (plant) must be a linear. So after some modulation the converter is modeled into a linear system for each of the switch options.

The controls implemented are PI, lead-lag and lag- lead and their graphs have been plotted.

II. Circuit And Operation

Flyback converter circuit diagram has shown in fig.1 and fig.2. The converter operates in two modes, mode 1 when the switch (MOSFET) is on and mode 2 when the switch (MOSFET) is off.

Mode 1: In this mode, MOSFET is on, positive side of the input supply is now connected to the primary winding of the transformer. While the potential induced in the secondary loop has opposite polarity than the primary loop and it causes the diode to get reverse biased and as a result diode doesn't allow current through it. Since only primary winding current is flowing, the flux is established in the transformer core completely due to input loop. This mode of circuit has been refereed here as Mode-1 of circuit operation. Fig.1 shows (in bold line) the current carrying part of the circuit and its functionally equivalent circuit during mode-1. In the equivalent circuit shown, the MOSFET is taken as a shorted switch and diode as open switch (assuming the switch (MOSFET) and diode to be ideal, having zero voltage drop during conduction and zero leakage current during off state).

Mode-2 starts when switch (MOSFET) 'S' is turned off after conducting for some time. The primary winding current path is broken since the switch 'S' is open and according to laws of magnetic induction, the voltage polarities across the windings get reversed. So now the diode in the secondary circuit is forward biased. Fig.2 shows the current path (in bold line) during mode-2 of circuit operation and its functional equivalent circuit during this mode.

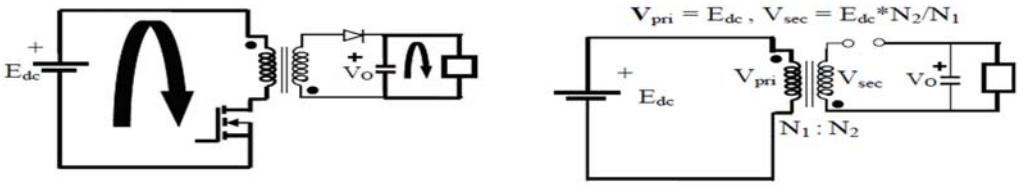

Fig. 1 Current path during Mode 1 and its equivalent circuit

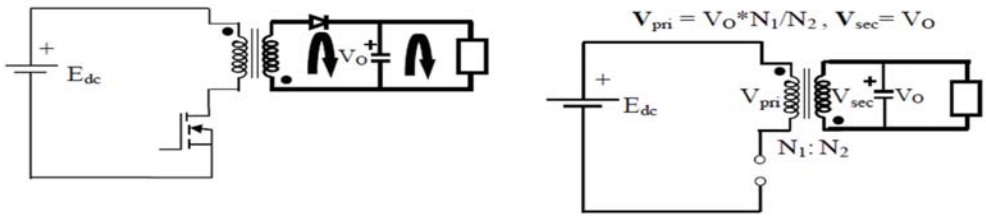

Fig. 2 Current path during Mode 2 and its equivalent circuit

III. Designing Of Flyback Converter

The converter was designed to have 5V dc output from 230V, 50Hz AC supply. The first step was to convert AC voltage to DC voltage, a rectifier circuit is used. Then unregulated DC voltage is filtered using a capacitor (called as link capacitor) and this output is given to a DC to DC converter, single ended isolated

flyback converter. The power MOSFET is used for the switching of the converter. Following is the complete design of the converter:

- Input min (minimum line voltage): 207V AC
- Input max (maximum line voltage): 253V AC
- Line frequency: 50 Hz
- Output power: 50W (5V, 10A)
- Inductor current ripple (δI_L): ± 10 % of 10A
- Output voltage ripple (δV_0): 2% of 5V
- Duty ratio (D): 0.45
- Current density (J): 3A/mm^2
- Flux density (B_{sat}): for Ferrite core: 0.3T
- Switching frequency (f_s) = 50 kHz

1) Power Calculation
Assume P_{in} = 62.5watts

2) DC link capacitor (C_{DC}):

C_{DC} = 2.5µF ∗ 62.5 = 156.25µF

3) $V_{DC})_{\min} = \sqrt{2 * (V_{line})_{\min}^{2} - \frac{P_{in}(1 - D_{ch})}{C_{DC} * f_L}} = 281.6V$

Where D_{ch} is Link capacitor charging ratio, typically about 0.2.

4) $V_{DC})_{\max} = \sqrt{2} * V_{line}^{\max}$

5) Primary side inductance (L_m):

$$L_m = \frac{((V_{DC})_{\min} * D_{\max})^2}{2 * P_{in} * f_s * K_{RF}} = 5mH$$

6) Transformer Design

a) Select transformer core: Ref. [1] for output power 30-50 watts select EE25 and for output power 50-70 watts select EE30. We are selecting here EE30.

b) Primary turns (NP):

$$N_P = \frac{(V_{DC})\max}{4 * B_m * (A_C)\text{selected} * f_s} = 215 turns$$

Bm is maximum operating flux, Bm = 0:25T

Ac)selected is selected core sectional area, Ac = 32mm^2

c) Turns ratio (n):

$$n = \frac{N_P}{N_S} = \frac{V_{RO}}{V_O + V_F} = \frac{230.4}{5 + 1} = 38.4$$

Where V_{R0} is voltage at primary transformer

V_o is output voltage

V_F is forward voltage drop of diode

d) Number of secondary turns (N^S) = 6

e) Output capacitor (C):

$$C = \frac{\delta I_L}{\delta V_C * 8 * f_S} = 25\mu F$$

Where δI_L is current ripple and δV_C is capacitor voltage ripple

7) Equivalent series resistance (R_C):

$$R_C = \frac{0.8 * \delta V_o}{\delta I_L} = 70m\Omega$$

IV. Small Signal Model Of The Converter

Ref. [2] switch mode DC to DC converters can be categorized as non-linear time-variant systems due to their inherent switching operation. The topology depends on instantaneous states of the power switches. This is what makes their modeling a complex task. Nevertheless, accurate analytical models of PWM DC to DC converters are essential for the analysis and design in many applications e.g., automobiles, aeronautics, aerospace, telecommunications, submarines, naval ships, and medical equipments.

Ref. [2, 7] the average-value modeling has been used very effectively for the system analysis and studies, wherein the effects of fast switching are neglected or averaged with respect to the switching interval. Continuous large-signal models are typically non- linear and can be linearized around a desired operating point. Averaged models of dc-dc converters offer several advantages over the switching models. Ref. [2] these advantages are: i) straight- forward approach in determining local transfer-functions ii) faster simulation of large-signal system-level transients and iii) use of general purpose simulators to linearize converters for designing the feedback.

To start converter dynamic modeling we first write down the dynamic as well as output equations for each of the switch positions in the converter. Fig.3 and fig.4 represents converter in mode 1 and mode 2 (without parasitic components) respectively while fig.5 and fig.6 represents converter in mode 1 and mode 2 (with parasitic components) respectively.

A. Small-Signal AC Model and State-Space Averaging without Parasitic in CCM

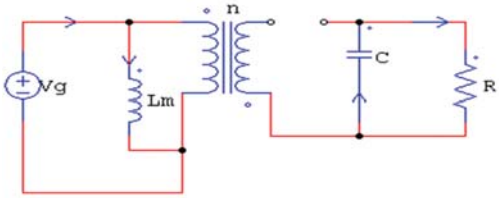

Fig. 3 Converter in Mode 1

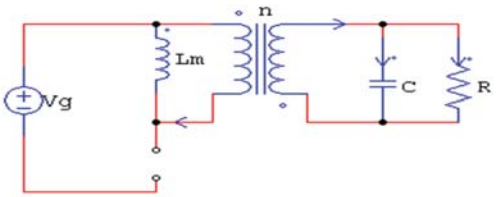

Fig. 4 Converter in Mode 2

- *MOSFET is ON and Diode is OFF*

$$v_g = v_L(t) \Rightarrow \frac{di}{dt} = \frac{1}{L_m} v_g \qquad (1)$$

Apply KVL in output loop

$$\frac{v(t)}{R} - i_C = 0 \Rightarrow \frac{dV_C}{dt} = \frac{1}{RC} v_C(t) \qquad (2)$$

And $v(t) = v_C(t)$ (3)

Where i_L and v_C are current through the primary side of inductance and voltage across capacitor respectively.

Ref. [3] integrator output values are taken as state variables since it can store past values as well. So i_L and v_C are taken as state variables (x).

$$A_1 = \begin{pmatrix} 0 & 0 \\ 0 & \frac{1}{RC} \end{pmatrix}, \; B_1 = \begin{pmatrix} \frac{1}{L_m} \\ 0 \end{pmatrix}, \; q_1 = (0 \; 1)$$

- *MOSFET is OFF and Diode is ON*

$$v_L = -n v_2 \Rightarrow \frac{di}{dt} = -\frac{n}{L_m} v(t) \qquad (4)$$

v_2 is voltage across secondary transformer which is equal to output voltage v(t) (where $v(t) = v_0$).

And

$$i_2 = n i_1 \qquad (5)$$

i_2 is current through secondary side of transformer and i_1 is current through primary side of transformer which also flows through Lm.

KVL in secondary loop

$$v_2 - v_C(t) = 0 \Rightarrow v_L = -[v_C(t)]n \qquad (6)$$

Using KCL

$$-n i(t) + i_C(t) + \frac{v(t)}{R} = 0 \Rightarrow \frac{dv_C}{dt} = \frac{n}{C} i(t) - \frac{1}{RC} v(t) \qquad (7)$$

KVL in output loop

$$v(t) = v_C(t) \qquad (8)$$

$$A_2 = \begin{pmatrix} 0 & -\frac{n}{L_m} \\ \frac{n}{C} & -\frac{1}{RC} \end{pmatrix}, B_2 = \begin{pmatrix} 0 \\ 0 \end{pmatrix}, q_2 = (0 \;\; 1)$$

Organizing all the above equations then the average state space model will be:

$A = A_1 d + A_2(1 - d)$

$B = B_1 d + B_2(1 - d)$

$q = q_1 d + q_2(1 - d)$

and $E = E_1 d + E_2(1 - d) = 0$

The dynamic equations are thus

$$\dot{x} = Ax + Bv_g \qquad (9)$$

$$v_o = qx + Ev_g \qquad (10)$$

Above equations are a large signal model of the system which represents the actual system. It has time varying'd' and therefore it is necessary to linearize the system equations. The obtained linearized model will allows us to define the different transfer functions for the converter and apply a linear system theory to design closed loop controllers for the converters. Small signal model gives us the idea of dynamics by deviation about operating point. Ref. [4] ideally the steady state gain is dependent only on the duty ratio (d) and independent of the switching frequency and load. Now consider that the inputs d and v_g are varying around their quiescent operating point D and Vg respectively.

$$d = D + \hat{d}$$

$$v_g = V_g + \hat{v}_g$$

d and v_g are time varying inputs and they are responsible for perturbations in the dynamic variables x (which are i_L and v_C) and v_o (where $v_o = v(t)$).

$$\dot{X} + \dot{\hat{x}} = A(X + \hat{x}) + B(V_g + \hat{v}_g) \qquad (11)$$

$$V_o + \hat{v} = q(X + \hat{x}) \qquad (12)$$

$$\dot{X} + \dot{\hat{x}} = [A_1(D + \hat{d}) + A_2(1 - D - \hat{d})](X + \hat{x}) + [B_1(D + \hat{d}) + B_2(1 - D - \hat{d})](V_g + \hat{v}_g) \qquad (13)$$

$$V_o + \hat{v}_o = [q_1(D + \hat{d}) + q_2(1 - D - \hat{d})](V_g + \hat{v}_g) \qquad (14)$$

The above equations may be expanded and separated into its dc (steady state part), linear small signal terms and non-linear terms. When the perturbations in d and v_g are small, the effect of nonlinear terms will be very small on the overall response and hence may be neglected (i.e $\hat{x} \cdot \hat{d} = 0$).

DC model:

$$0 = AX + BV_g$$

or

$$X = -A^{-1}BV_g \qquad (15)$$

$$\dot{\hat{x}} = [A_1\hat{d} - A_2\hat{d})]X + [B_1\hat{d} - B_2\hat{d}]V_g + [A_1D + A_2(1 - D)]\hat{x} + [B_1D + B_2(1 - D)]\hat{v}_g \qquad (16)$$

$$\dot{\hat{x}} = [A_1\hat{d} - A_2\hat{d})]X + [B_1\hat{d} - B_2\hat{d}]V_g + A\hat{x} + B\hat{v}_g \qquad (17)$$

$$\dot{\hat{x}} = A\hat{x} + B\hat{v}_g + f\hat{d} \qquad (18)$$

Where $f = [(A_1 - A_2)X + (B_1 - B_2)V_g]$

Similarly

$$\dot{\hat{v}}_o = q\,\hat{x} + [(q_1 - q_2)X]\,\hat{d} \qquad (19)$$

Input transfer function ($\hat{d} = 0$)

$$\frac{\hat{v}_o}{\hat{v}_g} = q(SI - A)^{-1}B \qquad (20)$$

Control transfer function ($\hat{v}_g = 0$)

$$\frac{\hat{v}_o}{\hat{d}} = q(SI - A)^{-1}f \qquad (21)$$

B. Small-Signal Model and State-Space Averaging with Parasitic in CCM

- *MOSFET is ON and Diode is OFF*

KVL in input loop

$$v_g(t) - v_L(t) - i(t)R_{sw} = 0 \Rightarrow \frac{di(t)}{dt} = \frac{v_g(t) - i(t)R_{sw}}{L_m} \qquad (22)$$

$$\frac{v(t)}{R} - i_C = 0 \qquad (23)$$

$$v(t) = \frac{R}{R + R_C} v_C(t) \qquad (24)$$

Using equation (24) in equation (23)

$$i_C = \frac{1}{R + R_C} v_C(t) \Rightarrow \frac{dv_C}{dt} = \frac{1}{(R + R_C)C} v_C(t) \qquad (25)$$

Where R_{sw} is internal resistance of MOSFET.
R_C is ESR of capacitor.
Lm is transformer primary side inductance.

$$A_1 = \begin{pmatrix} \frac{-R_{sw}}{L_m} & 0 \\ 0 & \frac{1}{(R + R_C)C} \end{pmatrix} \quad B_1 = \begin{pmatrix} \frac{1}{L_m} \\ 0 \end{pmatrix}, \quad q_1 = \begin{pmatrix} 0 & \frac{R}{R + R_C} \end{pmatrix}$$

- *MOSFET is OFF and Diode is ON*

$$v_L(t) = -nv_2 \qquad (26)$$

Where v_2 is voltage across secondary transformer

$$i_2(t) = ni(t) \qquad (27)$$

Where $i_2(t)$ is current through secondary transformer and $i(t)$ is current through L_m.
Using KVL in secondary transformer's loop

$$v_L = -n[v_C(t) + V_d + i_C(t)R_C] \qquad (28)$$

Where V_d is voltage across diode when it is on and v_L is voltage across L_m.

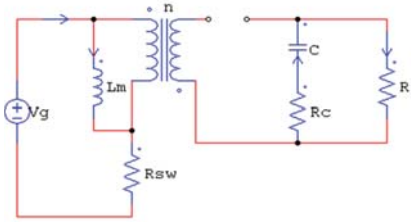

Fig. 5 Converter in Mode 1

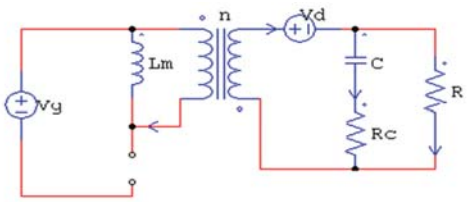

Fig. 6 Converter in Mode 2

Using KCL

$$i_C(t) = n\,i(t) - \frac{v(t)}{R} \qquad (29)$$

Applying KVL in output loop

$$v(t) = v_C(t) + i_C(t)R_C \qquad (30)$$

Put equation (30) in equation (29)

$$i_C = \frac{nR\,i(t) - v_C(t)}{R + R_C} \qquad (31)$$

Put equation (31) in equation (30)

$$v(t) = v_C(t)\frac{R}{R+R_C} + \frac{RR_C n}{R+R_C} i(t) \qquad (32)$$

From equation (28)

$$\frac{di}{dt} = -\frac{nR}{(R+R_C)L_m} v_C(t) - \frac{n^2 RR_C}{(R+R_C)L_m} i(t) - \frac{n}{L_m} v_d \qquad (33)$$

From equation (31)

$$\frac{dv_C(t)}{dt} = \frac{nR}{(R+R_C)C} i(t) - \frac{1}{(R+R_C)C} v(t) \qquad (34)$$

$$A_2 = \begin{pmatrix} \frac{-n^2 RR_C}{L_m(R+R_C)} & \frac{-nR}{L_m(R+R_C)} \\ \frac{nR}{C(R+R_C)} & \frac{-1}{(R+R_C)C} \end{pmatrix}, \quad B_2 = \begin{pmatrix} 0 \\ 0 \end{pmatrix}, \quad q_2 = \begin{pmatrix} \frac{RR_C n}{R+R_C} & \frac{R}{R+R_C} \end{pmatrix}$$

Organizing all the above equations then the average state space model will be:

$A = A_1 d + A_2(1-d)$
$B = B_1 d + B_2(1-d)$
$q = q_1 d + q_2(1-d)$
and $E = E_1 + E_2(1-d) = 0$

The dynamic equations are thus

$$\dot{x} = Ax + bv_g + nV_d \qquad (35)$$

Where V_d is passive switch ON state drop

$$v_o = qx + Ev_g \qquad (36)$$

Above equations are large signal model of the system which represents the actual system. It has time varying'd' and therefore it is required to linearize the system equations. If we get a linearized model we can define different transfer function for the converter and apply linear system theory which will help us to design closed loop controllers for the converters. Small signal model gives us idea of dynamics by deviation about operating point. Ideally the steady state gain is independent of the switching frequency and load, it depends only on the switching duty ratio. We may also neglect the terms containing V_d (passive switch on state drop) for this purpose. Ref. [4] this will be a valid step since these quantities are small (compared to Vg and V_o) .

Now we consider that the inputs v_g and d are changing around their quiescent operating point (Q- point) Vg and D respectively.

$d = D + \hat{d}$

$v_g = V + \hat{v}$

Inputs d and v_g are responsible to produce perturbations in the dynamic variables x (state variables) and v_o (output).

$$\dot{X} + \dot{\hat{x}} = A(\hat{X} + \hat{x}) + B(V_g + \hat{v_g}) + nV_d \qquad (37)$$

$$V_o + \hat{v}_o = q(X + \hat{x}) \quad (38)$$

$$\dot{X} + \dot{\hat{x}} = [A_1(D + \hat{d}) + A_2(1 - D - \hat{d})](X + \hat{x}) + [B_1(D + \hat{d}) + B_2(1 - D - \hat{d})](V_g + \hat{v}_g) \quad (39)$$

$$V_o + \dot{\hat{v}}_o = [q_1(D + \hat{d}) + q_2(1 - D - \hat{d})](V_g + \hat{v}_g) \quad (40)$$

Ref. [4, 8] the above equations may be further expanded and categorized into three separate terms named as DC (steady state part), linear small signal terms and non-linear terms. Nonlinear terms are product of two small terms so when the perturbations in d and v_g are small, the product will be very small and hence may be neglected (i.e $\hat{x}.\hat{d} = 0$).

On modulation and separation of small signal terms (linear terms, as we did in 'without parasitic' case) we get the small signal model.

$$\dot{\hat{x}} = A\hat{x} + B\hat{v}_g \quad (41)$$

$$\dot{\hat{v}}_0 = q\hat{x} + [(q_1 - q_2)X]\hat{d} \quad (42)$$

Where $f = (A_1 - A_2)X + (b_1 - b_2)Vg$

$$\frac{\hat{v}_o}{\hat{v}_g} = q(SI - A)^{-1}B \quad (43)$$

Equation (43) shows the amount of input variable that will reach the output as a function of frequency.

$$\frac{\hat{v}_o}{\hat{d}} = q(SI - A)^{-1}f \quad (44)$$

Equation (44) relates the gain between the control duty ratio and the output variable, $\frac{\hat{v}_o}{\hat{d}}$ called as control voltage gain.

TABLE I. SPECIFICATION OF CONVERTER

Input voltage(v_g)	146V
Duty ratio(d)	0.45
Load(R)	0.5Ω
Transformer turns ratio(n)	39
Transformer primary side inductance(L_m)	5mH
Output capacitor(C)	25μF
Equivalent Series resistance(R_C)	70mΩ
R_{sw}	1Ω

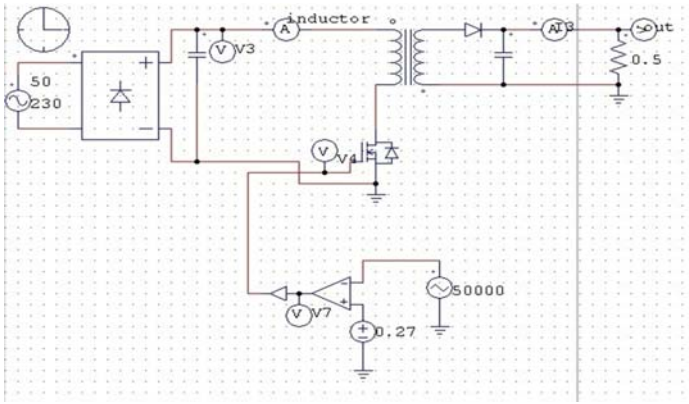

Fig. 7 PSIM model of flyback converter in open loop

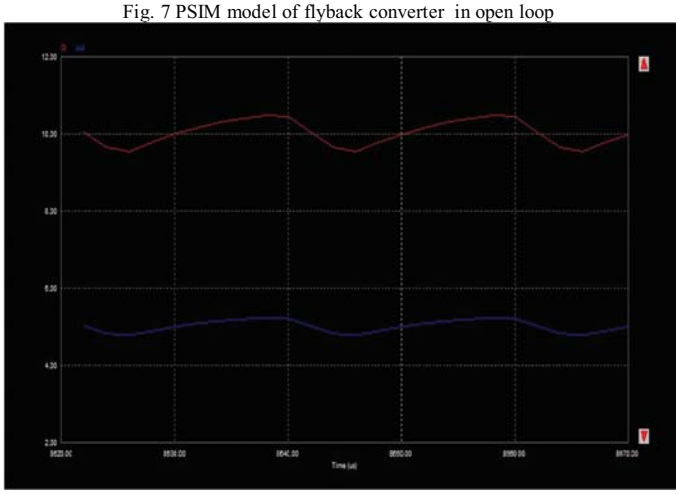

Fig. 8 Output voltage and current in open loop

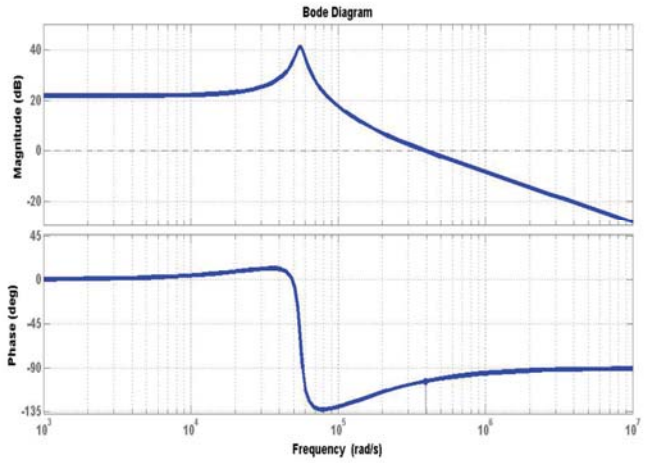

Fig. 9 Control voltage gain and phase plot without parasitic components

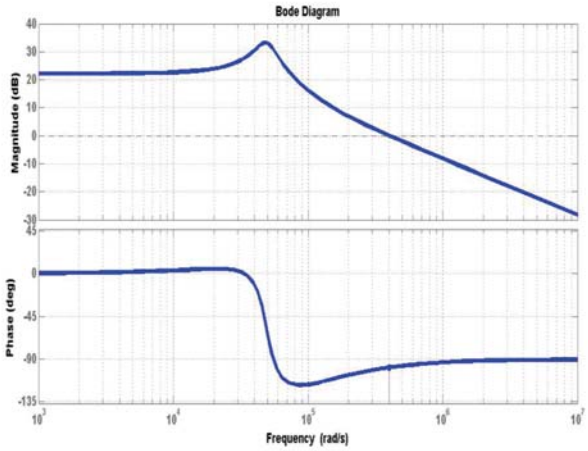

Fig. 10 Control voltage gain and phase plot with parasitic components

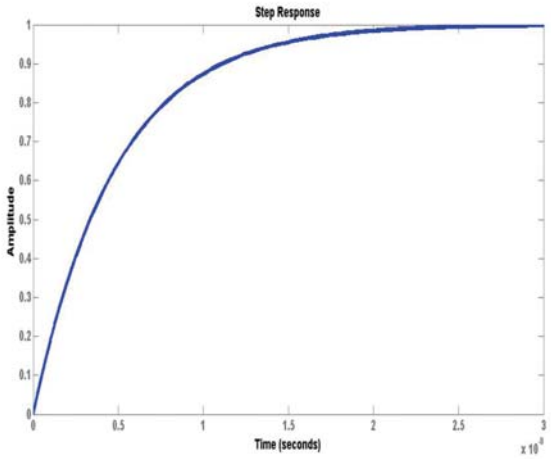

Fig. 11 Control voltage gain step response with PI controller (without parasitic)

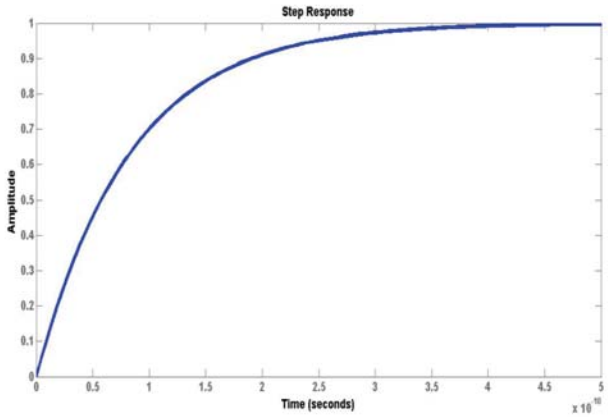

Fig. 12 Control voltage gain step response with PI controller (with parasitic)

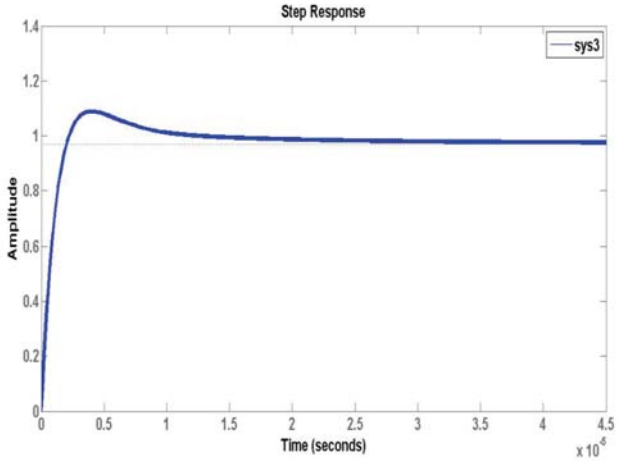

Fig. 13 Control voltage gain step response with lead lag compensator (without parasitic)

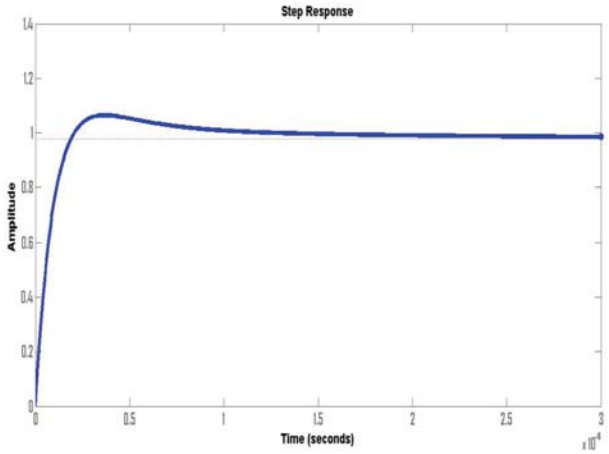

Fig. 14 Control voltage gain step response with lead lag compensator (with parasitic)

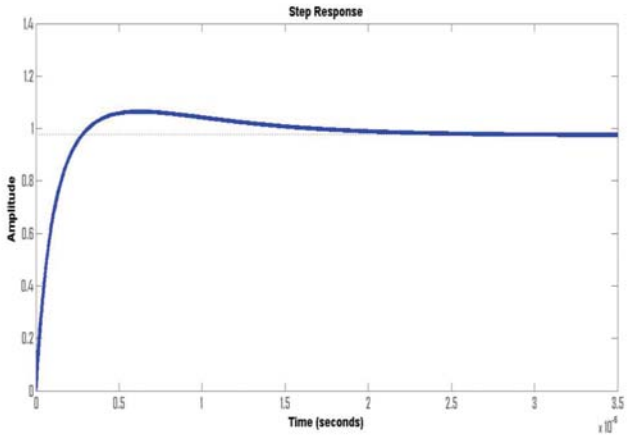

Fig. 15 Control voltage gain step response with lag lead compensator (without parasitic)

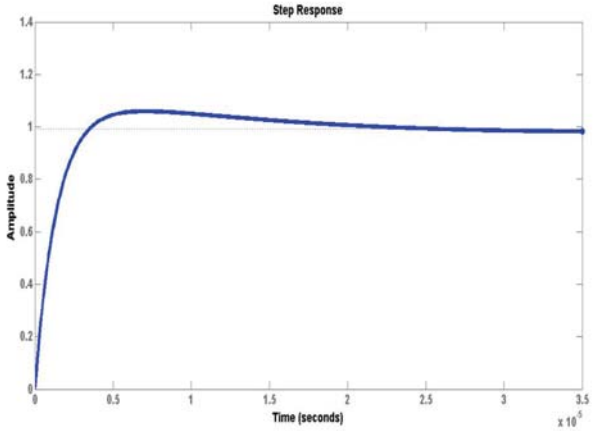

Fig. 16 Control voltage gain step response with lag lead compensator (with parasitic)

TABLE II. COMPARISON OF RESULTS

Controller/ Compensator	Without Parasitic	With Parasitic
PI	Phase margin= 90.3° Settling time= 6.28ms Peak overshoot= 0 Steady state error= 0	Phase margin= 90.5° Settling time= 2.8ms Peak overshoot= 0 Steady state error= 0.01
Lead lag	Phase margin= 79.8° Settling time= 7.4µs Peak overshoot= 0.09 Steady state error= 0.01	Phase margin= 81.5° Settling time= 8.1µs Peak overshoot= 0.07 Steady state error= 0.01
Lag lead	Phase margin= 88.4° Settling time= 0.17µs Peak overshoot= 0.08 Steady state error= 0.02	Phase margin= 73.6° Settling time= 8.91µs Peak overshoot= 0.1 Steady state error= 0.01

V. SIMULATION RESULTS

Flyback DC-DC converter has been simulated based on the developed design using PSIM6.0, specification of the converter has been given in the table 1. In this case, duty ratio is generated using op-amp. In order to evaluate the system's bode plot and their step response, it is simulated in MATLAB and then control strategies applied are 'PI', 'lead lag' and 'lag lead' for without parasitic as well as with parasitic components. Fig. 8 shows PSIM output in open loop. Fig. 9 and fig. 10 shows converter bode plot (in open loop) and from fig. 11 to fig. 16 show step response of the converter after implementing PI controller and Compensators. As it can be seen from table 2 that PI has more phase margin (in the range of 90°) as well as no overshoot while the compensators have phase margin in the range of 80°.

VI. CONCLUSIONS

Simple modeling method is presented which is based on the equivalent circuit of converter in on and off period. The developed model is simulated in MATLAB/Simulink software. Simulation result clearly shows that the system is stable and will give desired specifications when applied to the proper controller. We are getting steady state error less than 2% and phase margin more than 45°. Here we have applied three control strategies named as PI, lead - lag and lag - lead and their results have been compared. Although integral makes system slow but it doesn't allow any overshoot.

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